Amendments to the Claims

Please amend claims 1, 8, 9, 13. Please cancel claims 14-19 without prejudice. Applicant reserves the right to file these claims in a continuation or divisional application. The Claim Listing below will replace all prior versions of the claims in the application. No new matter has been added by way of these amendments.

Claim Listing

1. (Currently amended) A method of reducing data path latency in digitally processing a sequence of data samples, the data path latency being associated with a transient processing operation on the data samples, comprising:

    at the transition into the transient processing operation on the data samples reading the sequence of data samples into a tapped clocked delay chain, wherein each data storing element of the chain has an associated enabling signal for controlling, on any given clock cycle, whether to update or not its respective stored data sample;

    during the transient processing operation on the data samples, processing data samples from taps on the clocked delay chain; and

    in response to receiving a signal of completion of the transient processing operation on the data samples, controlling the enabling signal of each data storing element in the chain to allow shifting data samples rapidly out through an end portion of the clocked delay chain at a higher output rate on a selected first set of clock cycles determining a first shifting rate and than an input rate of data samples coming into the clocked delay chain shifting data samples in an initial portion of the delay chain on a selected second set of clock cycles determining a second shifting rate, wherein the initial portion is complementary to the end portion and wherein the first shifting rate is higher than the second shifting rate; and

    dynamically reducing the length of the clocked delay chain by moving the output of the delay chain to the last data storing element of the initial portion, after a number of clock cycles as data samples continue to be read into the clocked delay chain.

2. (Previously Presented) The method of Claim 1 wherein the data samples are from a data packet.

3. (Previously Presented) The method of Claim 2 wherein the data packet conforms to a transmission system selected from the group of 802.11a, 802.11g and HIPERLAN/2 transmission systems.

4. (Previously Presented) The method of Claim 3 wherein the transient processing operation includes a synchronization of the data packet.

5. (Previously Presented) The method of Claim 4 wherein the clocked delay chain comprises a plurality of pipelined registers.

6. (Previously Presented) The method of Claim 5 wherein the reducing the length of the clocked delay chain is performed until a desired length of the clocked delay chain is achieved.

7. (Previously Presented) The method of Claim 5 wherein reducing the length of the clocked delay chain further includes bypassing empty registers.

8. (Currently amended) A method of reducing data path latency in digitally processing a sequence of data samples of a data packet, the data path latency being associated with synchronization of the data packet, comprising:

upon reception of the data packet, reading the sequence of data samples from the data packet into a tapped clocked delay chain comprising a plurality of pipelined registers, wherein each register has an associated enabling signal for controlling, on any given clock cycle, whether to update or not its respective stored data sample;

processing data samples from taps on the clocked delay chain to synchronize the data packet;

in response to receiving a signal of completion of synchronization of the data packet, <u>controlling the enabling signal of each data storing element in the chain to allow</u> shifting samples ~~rapidly out~~ <u>through an end portion</u> of the clocked delay chain ~~at a higher output rate~~ <u>on a selected first set of clock cycles determining a first shifting rate and than</u> ~~an input rate of data samples coming into the clocked delay chain~~ shifting data samples <u>in an initial portion of the delay chain on a selected second set of clock cycles determining a second shifting rate, wherein the initial portion is complementary to the end portion and wherein the first shifting rate is higher than the second shifting rate</u>;

reducing the length of the clocked delay chain by <u>moving the output of the delay chain to the last register of the initial portion, after a number of clock cycles</u> ~~bypassing empty registers as data samples continue to be read into the clocked delay chain~~; and

repeating the steps of shifting data samples <u>through an end portion of the reduced delay chain and through the initial portion</u> ~~rapidly out of the clocked delay chain at a higher output rate than the input rate~~ and reducing the length of the clocked delay chain.

9.   (Currently amended) An apparatus comprising:

a pipeline of registers that store data samples;

logic circuitry which ~~controls~~ <u>allows</u> each individual register of the pipeline of registers <u>to be updated or not on any given clock cycle</u>;

a multiplexer having inputs from <u>outputs of</u> select<u>ed</u> <u>sections of</u> registers from the pipeline of registers, and an output; and

a processor which controls ~~the data shifting rates~~ , the logic circuitry, and the output of the multiplexer, <u>to allow</u> <u>for different</u> <u>data shifting rates</u> <u>through said selected sections, based on different selected sets of clock cycles</u> <u>and for a reduction in length of the pipeline of registers</u> ~~based upon~~ completion ~~states~~ of a transient processing operation on the data samples.

10.   (Original) An apparatus of Claim 9 wherein the data samples are from a data packet.

11.   (Previously Presented) The apparatus of Claim 10 data packet conforms to 802.11a, 802.11g and HIPERLAN/2 transmission systems standards.

12.　　(Original) An apparatus of Claim 11 further comprising a timing recovery module for synchronization of the data packet that initiates a transition in the processor.

13.　　(Currently amended) An apparatus comprising:

　　　　　a pipeline of registers that stores data samples of a data packet;

　　　　　a timing recovery module for synchronization of the data packet that initiates a transition;

　　　　　logic circuitry which ~~controls~~ allows each individual register of the pipeline of registers to be updated or not on any given clock cycle;

　　　　　a multiplexer having inputs from outputs of selected sections of registers from the pipeline of registers, and an output; and

　　　　　a processor having inputs from a timing recovery module for packet synchronization which controls ~~the data shifting rates,~~ the logic circuitry, and the output of the multiplexer to allow for different data shifting rates through said selected sections, based on different selected sets of clock cycles and for a reduction in length of the pipeline of registers ~~based~~ upon completion ~~states~~ of the synchronization of the data packet.

14-19. (Cancelled).

20.　　(Previously Presented) The apparatus of Claim 13 wherein the processor is a state-machine.